Monday 2004 Tutorials

Future CMOS	Gate Dielectrics	Low k/Cu Interconnects	RF/MMIC Reliability	Failure Analysis
201. Trends and Challenges in Device Scaling and Circuit Design D. Cox, IBM	211. Gate Oxide Reliability Methodology and Models R. Vollerston, Infineon	221. Low k/Cu Integration G. Dixit Applied Materials	231. Microwave/RF MMIC Rel. Physics and Test Methods J. Scarpulla Aerospace Corp.	241. Failure Analysis: Current Processes and Future Needs L. Wagner Texas Instruments
202. Future Direction & Challenges for Flash Memory Scaling G. Atwood/S. Lai Intel	212. Oxide BD in CMOS Devices and Circuits J. Stathis, IBM	222. Planarization for Cu/Low k Interconnects W.-Y. Hsu Applied Materials	232. MMIC Manufact. and Packaging Rel. Issues W. Roesch TriQuint	242. Failure Site Isolation Methods E. Cole Sandia Nat'l Labs & D. Vallett IBM Technology
203. Reinventing CMOS: Physics, Reliability, and the Roadmap T. Dellin Sandia National Laboratory	213. Multiple-BD Statistics & Post-BD Rel. Methodology J. Sune, U. Auto. Barcelona & E. Wu, IBM Microelectronics	223. Electromigration Reliability of Cu/Low k Interconnects P. Ho U.T. at Austin	233. SiGe & Si Base RF Technologies; Device Models & Characterization, Circuit & System Applications & Reliability Issues W. Abadeer, J. Walko, T. Bonaccio IBM Microelectronics	
	214. Rel. Issues on High-k Gate Diel. – What is Different from SiO_2 H. Satake et al. Toshiba	224. Via Stress Migration and Via Voiding G. Alers Novellus	234. HBT Reliability: Comp. SiGe, and III-V Heterojunction Bipolar Transistor Reliability F. Guarin IBM Microelectronics	