Sunday 2004 Tutorials

General Reliability	ESD	High K Dielectric	NBTI
101. Introduction to Reliability V. Reddy Texas Instruments	121-1. Latchup in CMOS Technologies S. Voldman IBM Microelectronics	131. Material Properties and Local Phenomena in High K Dieletrics G. Wilk ASM America	141. NBTI: Physics, Materials & Process Issues D. Schroeder Arizona State University
	121- 2. ESD in CMOS Technologies S. Voldman IBM Microelectronics	132. Interfacial Reactions and Stability of High K Dielectrics and Metals R. Wallace University of Texas, Dallas	142. NBTI: Device and Circuit Issues A. Krishnam Texas Instruments
Design Practices			**SER**
111. Product Reliability Challenges for VLSI Technology R. Bolam IBM Microelectronics	122. ESD Protection Design in CMOS T. Maloney Intel	133. Deposition & Defect Characterization of High K Material J. Conley Sharp	151. Introduction to SER and Testing Challenges R. Velasco TIMA
112. Effects of Reliability Mechanisms on VLSI Circuit Functionality W. Ellis IBM Microelectronics	123. ESD Testing: HBM to vf-TLP H. Gieser Fraunhofer IZM	134. Defect Transport of High K Dielectrics E. Cartier IBM Semiconductor Research and Development Center	152. Software Approaches to Mitigating SERs F. Faure TIMA
			153. Simulation Techniques for FPGA Soft-Errors M. Wirthlin, BYU