IRPS 2013

IEEE International Reliability Physics Symposium

Sunday Tutorial Presentations

April 14, 2013

S1.1: III-V Device Characterization
S1.2: Monte Carlo Methods in Reliability Physics
S1.3: Fundamentals of RTN, BTI, and Hot Carrier Degradation: A Matter of Timescales
S1.4: Fundamentals of Dielectric Breakdown Reliability
S2.1: Reliability Physics of High-k/Metal Gate Stacks for Advanced CMOS Technology
S2.2: Metal Gate/High-k Bias Temperature Instability: Characterization and Modeling
S2.3: High-k / Metal Gate 3 (TDDB)
S2.4: Emerging Middle-of-line Reliability Issues
S3.1: In-Situ Monitoring of Reliability in Circuits
S3.2: Reliable systems from unreliable components: Resilient and adaptive circuits
S3.3: Starter Kit for Chip-to-System Reliability
S3.4: Design for Reliability
S4.1: Flash Reliability
S4.2: Emerging Memory Technologies
S4.3: On the Intrinsic Variability and Reliability of Solar Cells

Sunday Tutorial Topic 1.1

III-V Device Characterization

Suman Datta, Penn State University

Abstract

In this tutorial, I will introduce the scaling challenges facing Silicon MOSFETs. I will discuss how III-V MOSFETs can address scaling as well as energy efficiency needs of future devices. Amongst many challenges that need to be overcome for III-V MOSFETs, demonstration of a high quality high-k / III-V interface remains a primary one. Various characterization techniques to understand III-V/high-k interface will be discussed. Finally, we will end with a discussion on the current status of multi-gate III-V MOSFETs and their electrical performance.

About the Author

Suman Datta is Professor of Electrical Engineering at the Pennsylvania State University, University Park. Datta received his degrees in Electrical Engineering, attending IIT Kanpur and University of Cincinnati. After working at Intel Research for eight years, he joined Penn State in 2007. He is exploring novel classical and non-classical device architecture for CMOS "enhancement" and CMOS "replacement" for future energy efficient computing applications. Datta is a Fellow of IEEE and Distinguished Lecturer of the IEEE Electron Devices Society. He received the 2012 IBM Faculty Award and the 2012 Penn State Engineering Alumni Society Outstanding Research Award. He received the 2012 SEMI Award for North America and the 2003 Intel Achievement Award with his former colleagues at Intel for contribution to high-k/metal gate CMOS transistor research. He has authored over 140 refereed journal and conference publications and holds 150 US patents related to transistor innovation. He can be reached at sdatta@engr.psu.edu

Sunday Topic 1.2

Monte Carlo Methods in Reliability Physics

John W. Evans, NASA

Abstract

Monte Carlo (MC) simulation is a highly effective technique to support reliability analyses. The technique is often misunderstood as an overly complex and time consuming approach to generating a probabilistic analysis. In fact, MC simulation is conceptually simple and can be very useful in developing an understanding of the impact of variations in materials properties, design parameters and manufacturing processes on the reliability of components and systems. Many problems are readily implemented into a simulation with relatively simple programming code, Excel based spreadsheets or by using existing commercial tools to drive the simulation. All are enabled by low cost computing capability.

The Monte Carlo simulation is a sampling technique that is used to propagate uncertainties in parameters that comprise a physical or economic system. Statistical distributions of parameters of interest are developed as inputs to the simulation process. Uniformly distributed random numbers are generated along the interval 0 to 1, allowing for repeated sampling of the input distributions. The sampled information is then used to exercise an otherwise deterministic model that represents the system under study. The results are accumulated for the desired number of samples and analyzed. Basic statistics or probabilities of the possible outcomes may be determined from the final analysis. Hence, the simulation enables "explicit treatment of the uncertainties" rather than focusing on deterministic results.

This tutorial will introduce the concepts of Monte Carlo simulation and how it can be applied to support assessments that reliability and maintainability professionals apply to assess failure processes impacting the design and manufacturing of systems. The tutorial will cover setting up the analysis, implementation and interpretation of the results. In addition, a basic process for modeling failures will be presented. The remainder of the tutorial will center on pragmatic examples to include the development of reliability centered quality criteria for inspection purposes, development of strength distributions for probabilistic design and assessment of wear out processes, including examples in fatigue and corrosion. Emphasis is placed on electronic products. However, the concepts presented will enable engineers, in many market segments to employ this technique successfully.

About the Author

Dr. John W. Evans is currently a senior NASA Engineer working on the development of the James Webb Space Telescope and other NASA projects including the Magnetospheric Multiscale Mission at the Goddard Space Flight Center. He is responsible for reliability analysis and risk assessment. Dr. Evans has over 30 years of experience and has held positions in industry and academia. He has been a consultant to major companies worldwide, having worked in 10 different countries. He has authored or coauthored 3 textbooks, a book chapter on electronic materials and over 50 publications. He holds his Ph.D in Materials Science and Engineering from Johns Hopkins University, MS in Chemical and Materials Engineering from the University of Iowa and BS from University of Nebraska in Mechanical Engineering. Dr. Evans is also serving as an Adjunct Professor in the Department of Industrial and Systems Engineering at the Morgan State University in Baltimore.

Sunday Tutorial 1.3

Fundamentals of RTN, BTI, and Hot Carrier Degradation: A Matter of Timescales

Tibor Grasser, Technische Universitaet Wien

Abstract

Even under stationary bias conditions, fluctuations in the terminal currents of MOSFETs can be observed, a phenomenon which has become known as random telegraph noise (RTN). The magnitude of these fluctuations increases with decreasing device area. The commonly accepted interpretation explains the noise as a result of stochastic trapping of charge carriers into oxide or interface defects. Experimental data show that the average capture and emission times of this trapping process exhibit pronounced temperature and bias dependencies.

Of particular importance is the exponential bias dependence of the capture times, which naturally links RTN to the bias temperature instability (BTI): application of large electric fields results in a dramatic decrease of the capture times, thereby upsetting the dynamic equilibrium typical for RTN. Since the defects present in a MOSFET have a wide distribution of time constants, not all defects capture their charge at the same time. Rather, one defect after the other captures its charge, resulting in slow drifts in the terminal characteristics of the MOSFET. The opposite is observed once the stress field is removed, producing long recovery transients. In nanoscale MOSFETs these degradation and recovery transients proceed in discrete steps, with each step being due to charge exchange of a particular defect with the substrate or the gate. A somewhat more complicated phenomenon is hot carrier degradation, where the above time constants now also depend on the current flowing through the channel.

While the chemical nature of the defects contributing to these various detrimental phenomena is still not fully understood, one unifying feature seems to be inherent in all of them: the wide distribution of the timeconstants, covering many decades in time. As a consequence, many features of these degradation phenomena can be understood by studying the distribution of these timeconstants, an issue which will be discussed in depth.

About the Author

Tibor Grasser received his Ph.D. degree in technical sciences from the TU Wien where he is currently employed as an Associate Professor. In 2003 he was appointed director of the Christian Doppler Laboratory for TCAD in Microelectronics. Dr. Grasser is the co-author or author of more than 400 scientific articles, editor of a book on advanced device simulation, a distinguished lecturer of the IEEE Electron Devices Society, a senior member of IEEE, has been involved in various functions of outstanding conferences such as IEDM, IRPS, SISPAD, IWCE, ESSDERC, IIRW, and ISDRS, is a recipient of the Best Paper Awards at IRPS (2008 and 2010), ESREF (2008) and the IEEE EDS Paul Rappaport Award (2011). He was also a chairman of SISPAD 2007.

Sunday Tutorial Topic 1.4

Fundamentals of Dielectric Breakdown Reliability

Ernest Wu and Jordi Suñé*

IBM Semiconductor Research and Development Center
Universitat Autonoma de Barcelona

Abstract

Dielectric breakdown reliability has faced new challenges with the introduction of new materials such as high-κ and low-κ dielectrics and with multiple failure modes due to ever increased process and geometric and/or structural complexities. Meanwhile, the requirements for fast turn-around TDDB evaluation and qualification in order to reduce product costs with the same or more stringent reliability specifications become more urgent than ever. These demands require a thorough understanding of the involved statistics of failure and should also be preferably based on a detailed knowledge of the physics involved. This tutorial is divided into three parts. In the first one, after a review of the basics of statistics and characterization techniques, we will present the methodologies required to model multiple breakdown-modes dealing with either the competition or the superposition of these different modes. Then, we will discuss the fact and myth surrounding the ramped voltage stress (RVS) methodology for fast turn-around TDDB assessments. In the second part, we will review the percolation model and its prediction in terms of thickness scaling. Moreover, several voltage acceleration models will be reviewed with emphasis on the hydrogen release-reaction model in the framework of two step defect generation processes. This model provides a plausible theoretical basis to the nowadays widely accepted power-law voltage acceleration model which is also found in both high-κ and low-κ dielectrics. Thirdly, we will review different approaches to the post-breakdown failure statistics but we will focus on recent advances related to the statistical description and experimental characterization of the progressive breakdown failure, including the case of multiple breakdown competition. At the end of this tutorial, we will show how the understanding of post breakdown can lead us to a more quantitative understanding of product faults such as SRAM circuit failure.

About the Authors

Ernest Y. Wu is a senior technical staff member at Semiconductor Research and Development Center (SRDC) in IBM Microelectronics Division. He is responsible for technology qualification and development of dielectric reliability methodologies. Dr. Wu has served on the device dielectric committee as chair and co-chair for 2007 and 2005 International Reliability Physics Symposium (IRPS), respectively. He is a member of CMOS and Interconnect Reliability committee of International Electron Device Meeting (IEDM) for 1999 and 2000. He has authored and co-authored more than 100 papers in technical journals and international conferences with several invited papers and tutorials as well as 15 IEDM papers. He has co-authored two books on gate dielectric reliability entitled “Reliability Wearout Mechanisms in Advanced CMOS Technologies” and “Defects in Semiconductors”. In 2004, he received IBM Outstanding Technical Achievement Award for contributions to ultra-thin gate reliability in advanced CMOS technology. His research interests include dielectric reliability physics, device physics and simulation.

Jordi Suñé is Professor at the Universitat Autònoma de Barcelona (UAB) since 2002. He has (co)authored more than 280 technical papers, among which 13 IEDM papers and 5 tutorials on oxide reliability at IRPS. In 2010 he was upgraded to IEEE Fellow for contributions to the understanding of gate oxide failure and reliability methodology. He coordinates the NANOCOMP research group which is dedicated to the characterization, modeling and simulation of electron transport in electron devices with a multi-scale approach that ranges from first-principle simulations to compact modeling. His main interests are oxide reliability and resistive switching devices for RRAM.

Sunday Tutorial Topic 2.1

Reliability Physics of High-k/Metal Gate Stacks for Advanced CMOS Technology

Eduard Cartier, IBM

Abstract

The transition from CMOS technologies with thermally grown SiO_2(SiON)/poly-Si based transistors to CMOS technologies with deposited high-k/metal-gate (HKMG) stacks is completed, and advanced CMOS technologies beyond the 45 nm node are largely based on HKMG transistors. While the introduction of HKMG enabled the continuation of CMOS scaling, the use of deposited dielectrics with high dielectric constant, k, in combination with deposited metal electrodes also brought about additional, new reliability challenges for CMOS technology reliability qualification, previously not encountered with conventional poly-Si/SiON gate stacks.

In this tutorial, the reliability challenges with HKMG dielectrics will be discussed in detail. It will be shown that with HKMG technologies, the positive bias temperature instability (PBTI) and stress-induced leakage currents (SILC) in nFET devices need to be qualified in addition to the much studied negative bias temperature instability (NBTI) in pFETs. Both of these instabilities have been of little importance for conventional transistors.

This tutorial will start with a 'historic' look at the transition from conventional to HKMG gate stacks with a focus on the importance of process optimization for reliability. The various factors such as the extreme oxygen sensitivity of the gate stack, will discussed in detail. Next, the basic electrical characterization of HfO_2/TiN gate stacks (the preferred stack in the industry), and the connection between the electrical response and the electronic and structural properties of HKMG stacks will be developed, resulting in a comprehensive semi-quantitative understanding of the charge transport and of the NBTI, PBTI, (and SILC) phenomena in HKMG transistors. In the final section, the appearance of a "reliability cliff" with continued HKMG scaling will be discussed and the emerging challenges for the continued use of HKMG dielectrics will be discussed and some recent advances in expanding the scalability of HKMG stacks from a reliability perspective will be addressed.

About the Author

Eduard A. Cartier earned his MS and PhD degrees in physics (Dr. sc. nat., with honors) from the Laboratory for Solid State Physics at the Swiss Federal Institute of Technology in Zurich (ETH), Switzerland, for his work on the electronic structure and on point defects in amorphous and synthetic metals, and in insulators. He received a grant for the promotion of Industry-University collaborations from the Swiss National Science Foundation to work from 1986 to 1988 at the ABB Research Center in Baden-Dättwil, Switzerland, on the contribution of hot carrier transport in wide band gap insulators to dielectric wear-out and breakdown in polymers insulations used for high power underground cables. In 1989, he joined the IBM Research Division at the T.J. Watson Research Center in Yorktown Heights, NY, USA as a research staff member, where he continues to work today.

Dr. Cartier's initial research activities at the T.J. Watson Research Center concentrated around hot carrier transport in silicon and silicon dioxide and around hot carrier induced oxide degradation and its impact on transistor stability and reliability in CMOS technologies and memory device. In 1998, he started with the development of deposited dielectrics with high dielectric constants to replace thermally grown SiO_2 as a gate insulator in field effect transistors, leading to some of the earliest demonstrations of HK/poly-Si and HK/MG short channel transistors for advanced CMOS technologies. Over the last 15 years, he was heavily involved in all aspects of gate stack development from basic research to technology qualification for the IBM HKMG technologies from the 45 to 7 nm node.

Dr. Cartier is coauthor of over 30 patents on the use of high-k dielectrics and metal gates in CMOS and memory technologies and he has published his work in over 100 contributions to peer reviewed journal, to conference proceedings of topical conferences (IEDM, VLSI, IRPS, INFOS, SISC, AVS and MRS) and in several chapters for topical books. He has made key contributions to the understanding of the fundamental gate stack properties, such as the understanding of the role of oxygen vacancies for the threshold voltage control and the stability of high-k/metal gate transistors. He continues to be involved in fundamental research on HKMG stacks, while he is also directly involved in the reliability qualification of IBM's emerging high-k/metal gate CMOS technologies.

Sunday Tutorial Topic 2.2

Metal Gate/High-k Bias Temperature Instability: Characterization and Modeling

Andreas Kerber, GLOBALFOUNDRIES

Abstract

The transition from poly-Si/SiON to Metal Gate/High-k stacks in CMOS technology has introduced additional challenges for reliability characterization and modeling of advanced transistor nodes. In addition to the negative bias temperature instability (NBTI) in pFET devices well known from poly-Si/SiON stacks, positive bias temperature instability (PBTI) and stress-induced leakage currents (SILC) in nFET devices have emerged as new degradation mechanism for MG/HK CMOS technologies.

This tutorial intends to provide an overview of the different characterization methods developed throughout the years to study various aspects of BTI. We discuss the impact of recovery effects on BTI modeling and projection. Furthermore we elaborate on the stochastic nature of BTI in small area devices and emphasize its growing importance for future CMOS generations. Finally we highlight the need for fast quantitative reliability screening procedures during the research and early development phase of advanced CMOS technologies.

About the Author

Andreas Kerber was born in Schnann, Austria, and received his Diploma in physics from the University of Innsbruck, Austria, in 2001, during which time he was working at Bell Laboratories, Lucent Technologies (Murray Hill, NJ, USA) on the electrical characterization of ultra-thin gate oxides. In 2001, he joined Infineon Technologies in Munich, Germany. From 2001 to 2003, he was assigned to International SEMATECH at IMEC in Leuven, Belgium, where he was involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. At the same time he fulfilled the requirements for a PhD in electrical engineering and defended his thesis at the TU-Darmstadt, Germany, with honors. From 2004 to 2006, he was with the Reliability Methodology Department at Infineon Technologies in Munich, Germany, responsible for the dielectric reliability qualification of process technology transfers of 110 and 90 nm memory products. At the same time he developed a fast wafer-level data acquisition setup for time-dependent dielectric breakdown (TDDB) testing with sub-ms time resolution. In 2006, he joined AMD and now is with GLOBALFOUNDRIES in Yorktown Heights, NY, working as a Senior Member of Technical Staff on front-end-of-line (FEOL) reliability research with focus on metal gate / high-k CMOS process technology, advanced transistor architecture and device-to-circuit reliability correlation.

Dr. Kerber has contributed to more than 80 journal and conference publications and presented his work at international conferences, including the VLSI Technology Symposium, the International Electron Device Meeting (IEDM) and the International Reliability Physics Symposium (IRPS). In addition, he has presented invited talks at the Workshop of Dielectrics in Microelectronics (WoDIM), the Semiconductor Interface Specialist Conference (SISC) and given tutorials on metal gate / high-k reliability characterization at the International Integrated Reliability Workshop (IIRW) and IRPS. Dr. Kerber has served as a technical program committee member for the SISC (2006, 2007), IRPS (2007, 2011, 2012), IEDM (2011, 2012) and Infos (2013).

Sunday Tutorial Topic 2.3

High-k / Metal Gate 3 (TDDB)

Thomas Kauerauf, imec

Abstract

Planar CMOS device scaling required a continues reduction in the gate dielectric thickness. But around a thickness of 1.5nm the tunneling current through SiO2 is too high, reaching the device limits in terms of power dissipation and power consumption. Therefore alternative dielectrics with higher dielectric constant were introduced. This higher dielectric constant allows for physically thicker layers reducing the tunneling current, while at the same time the gate capacitance still can be increased. In this tutorial, an overview of time-dependent dielectric breakdown (TDDB) in high-k / metal gate stacks is given. TDDB is one of the main reliability concerns of CMOS logic devices, where the generation of defects leads to conductive paths though the dielectric and eventually to complete loss of the insulating properties. Since a typical high-k gate stack for logic devices consists of (at least) two layers, a few A thick SiO2 interface and a few nm thick high-k, and also different metal electrodes for nMOS and pMOS devices are used, we discuss the polarity dependence in terms of leakage current and the degradation during electrical stress. We then give some background on TDDB measurements using constant voltage stress and the TDDB lifetime extrapolation procedure. We further elaborate on the multiple stages in dielectric breakdown, namely soft breakdown, wearout and hard breakdown. While already just triggering on SBD is very challenging, we show that the SBD lifetime extrapolation results in insufficient reliability. Wearout and HBD have to be considered for the extrapolation and we present a model which includes all stages. Finally voltage ramp stress is discussed, providing a viable alternative to constant voltage stress especially for automated testing.

About the Author

Thomas Kauerauf was born in Leipzig, Germany. He received the degree in electrical engineering with the specialization in microelectronics and sensors from the TU Ilmenau, Germany, in 2001. From 1999 to 2000 he stayed for a 9 months internship at Bell Laboratories, Murray Hill, USA. He received the Ph.D. degree from the KU Leuven, Belgium, in 2007 on “Degradation and breakdown of MOS gate stacks with high permittivity dielectrics”. In 2006 he joined imec, Leuven, Belgium, working on the electrical characterization and reliability of high-k gate stacks, and the impact of Cu contacts on the FEOL reliability. He is currently the Team leader of the FEOL reliability team focusing on logic device, MOL and 3D architecture reliability. Thomas Kauerauf has authored or co-authored more than 100 international publications and served as a technical program committee member of IRPS.

Sunday Tutorial Topic 2.4

Emerging Middle-of-line Reliability Issues

Fen Chen
IBM Microelectronics

Abstract

Middle-of-Line (MOL) dielectric breakdown in advanced CMOS technology nodes has emerged as one of the most challenging reliability mechanisms due to the aggressive shrinking of the gate to diffusion contact pitch. Complicated process control such as PC-CA overlay, critical dimension (CD), and line-edge roughness (LER), rapid adoptions of new materials such as metal gate, stress liner, and copper contact, together with new device configurations such as epitaxial source/drain and FinFET could further exacerbate the PC-to-CA dielectric breakdown problem. Elevated PC-to-CA leakage and early breakdowns could result in product yield loss and functional stress failure if MOL process is not optimized. In this tutorial, how to conduct a comprehensive investigation of MOL PC-to-CA reliability, including novel testing structure design, new data analysis technique, and new qualification methodology will be introduced. Based on extensive wafer-level stress and product level stress data, it was found that multiple PC-to-CA failure modes could exist and act in concert or separately to determine the ultimate product reliability. Since various extrinsic defects convoluting together with spacing variation could severely impact PC-to-CA reliability data analysis, an accurate assessment of PC-to-CA dielectric reliability becomes extremely challenging. In this tutorial, various intrinsic PC-to-CA geometry induced failure modes and various process issue induced extrinsic failure modes will be discussed in details. It will be emphasized in this tutorial that both intrinsic minimum insulator spacing and extrinsic defects should be carefully evaluated during technology qualification in order to ensure a robust PC-to-CA reliability at product level.

About the Author

Fen Chen received his Ph.D. degree in Electrical Engineering in 1998 from University of Delaware. From 1997 to 1998, he was with IBM System Group at Rochester, MN and Intel Component Research at Santa Clara, CA as a graduate intern working on system stress and IC interconnect reliability. He joined IBM microelectronics at Essex Junction, VT in 1998 and has worked on semiconductor technology reliability issues since that time. During the past several years he has focused on low-k ILD TDDB and MOL PC-to-CA reliability issues for various IBM and IBM Alliance development programs at 65nm, 45nm, 32nm, 22nm, 20nm, and 14nm. He holds more than 30 patents and has published over 50 technical papers.

Sunday Tutorial Topic 3.1

In-Situ Monitoring of Reliability in Circuits

Chris H. Kim, University of Minnesota – Twin Cities

Abstract:

Device aging mechanisms such as Bias Temperature Instability (BTI), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB) have become serious problems undermining the long term reliability of high performance systems. In this tutorial, I will cover some of the latest research on in-situ circuit reliability monitoring techniques. This new class of compact on-chip sensors can reveal important aspects of circuit aging that would otherwise be impossible to measure using traditional device probing. Topics will range from high precision BTI monitors and dedicated circuits for separating the different aging mechanisms to SRAM reliability macros and TDDB characterization arrays.

About the Author

Chris H. Kim received his B.S. and M.S. degrees from Seoul National University and a Ph.D. degree from Purdue University. He spent a year at Intel Corporation where he performed research on variation-tolerant circuits, on-die leakage sensor design and crosstalk noise analysis. He joined the electrical and computer engineering faculty at the University of Minnesota in 2004 where he is currently an associate professor.

Prof. Kim is the recipient of an NSF CAREER Award, a Mcknight Foundation Land-Grant Professorship, a 3M Non-Tenured Faculty Award, DAC/ISSCC Student Design Contest Awards, IBM Faculty Partnership Awards, an IEEE Circuits and Systems Society Outstanding Young Author Award, ISLPED Low Power Design Contest Awards, and an Intel Ph.D. Fellowship. He has authored or co-authored more than 100 journal and conference papers and has served as a technical program committee member for a number of circuit design conferences. His research interests include digital, mixed-signal, and memory circuit design for silicon and non-silicon (organic TFT and spintronics) technologies.

Sunday Tutorial Topic 3.2

Reliable systems from unreliable components: Resilient and adaptive circuits

Jim Tschanz, Intel

Abstract

Today's microprocessor and SoC designs are used in an ever-increasing variety of systems and form factors with widely varying requirements on performance, workloads, and power consumption. These devices experience dynamic variations such as power supply fluctuation, temperature change, and transistor degradation that can cause failures if not properly accounted for at design time. At the same time, the necessity of ensuring correct operation even in the presence of these worst-case variations can result in large performance or power penalties. In this tutorial I will describe the impact of static and dynamic variations on the power and performance of digital logic, and explore several techologies for intelligently detecting and adapting to these variations. With these advanced "resilient" circuit techniques, even real timing errors can be detected and corrected, allowing reliable operation in the presence of multiple types of variations.

About the Author

Jim Tschanz received the B.S. degree in computer engineering and the M.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign, in 1997 and 1999, respectively. Since 1999, he has been a circuits researcher with the Intel Circuit Research Lab in Hillsboro, OR, where his research interests include low-power digital circuits, design techniques, and methods for tolerating parameter variations. He also taught VLSI design for 7 years as an adjunct faculty member at the Oregon Graduate Institute in Beaverton, OR. He has published 53 conference and journal papers in this field, has authored 3 book chapters, and has over 41 issued patents.

Sunday Tutorial Topic 3.3

Starter Kit for Chip-to-System Reliability

Mohammad Tehranipoor, Nematollah Bidokhti, Bill Eklow
University of Connecticut, Cicso Systems

Abstract

For a long time reliability has been an afterthought but with technology scaling, power, thermal, speed, complexity, time-to-market and cost there will be a significant impact on device and product reliability going forward. Given this "perfect technology storm" it is imperative today that engineers understand the impact of these influences on product reliability and become more proactive in identifying and addressing reliability risks in the design. The engineers/companies that are reactive will pay significantly, not only in terms of dollars but also in terms of customers.

This tutorial will cover the concepts around component and system reliability, including: definition of key terms, current and future challenges in reliability, tools, methodologies and processes for identifying reliability risks, case studies demonstrating problems and solutions.

This tutorial is perfect for participants who are either beginners or have been a reliability engineering background and require additional refresher with the latest development in area of design for reliability. Also, it is a great course for people who are interested in the field of reliability and robust design. It provides up-to-date understanding of next generation reliability and verification challenges and best practices. We will present (i) novel methodologies to analyze reliabilities at different levels (chip-to-system), (ii) case studies to help understand the impact oftechnology scaling and system complexity on reliability, (ii) pre-tapeout methodologies to perform better margining, and (iv) post-silicon self-healing and calibration methodologies.

In addition, the tutorial will include the current and future potential areas for reliability automation and robustness. The attendee will come out of the tutorial with a better understanding and a set of tools to proactively mitigate any reliability risks.

About the Authors

Nematollah Bidokhti is a Staff Engineer with Cisco Systems and a Research Specialist with ECE department in University of Connecticut. In Cisco, he leads the Design for Reliability (DFR) program. He has architected Cisco hardware& software DFR methodologies and responsible for DFR strategy and roadmap. He is leading various DFR initiatives in areas of ASIC, board and systems designs. His background includes hardware, software, system reliability engineering & modeling and Fault management. He holds a BSEE from Florida Atlantic University.

Mohammad Tehranipoor is an Associate Professor of ECE at the University of Connecticut. He is a recipient of a several best paper awards and the 2009 NSF CAREER award. He serves on the program committee of several leading conferences and workshops. He served as Program Chair and General Chair of several conferences and workshop. He is a Senior Member of the IEEE and Member of ACM and ACM SIGDA.

Bill Eklow is a Distinguish Manufacturing Engineer with Cisco Systems, responsible for "Chip to System" DFT and Test. Bill has been involved with chip, board and system DFT and test for over 30 years. He is an IEEE Senior Member, a Golden Core Member and Eta Kappa Nu member. He is chair of the IEEE 1149.6 working group and an inaugural member of the IEEE P1687 (IJTAG) working group. He has published over 20 papers.

Sunday Tutorial Topic 3.4

Design for Reliability

Vincent Huard, STMicroelectronics

Abstract

For many decades, IC component reliability relies on a top-down approach. In this approach, various elements of the product's mission profile were translated into reliability specifications at component level.

Nevertheless, this approach presents limitations in generating reliability specifications for the IPs or elementary blocks of the component.

These limitations become even more important to overwhelm with the continuous technology scaling and its related increase of the reliability impact.

For that purpose, lots of RnD work have been published over the last years regarding a bottom-up approach. In this approach, the reliability is dealt at design level from the beginning.

In a first time, the top-down approach and its limitations will be reviewed. From that status, this tutorial will introduce the bottom-up approach and will provide the key elements (and related examples) to focus on to build products accordingly to a Design For Reliability (DFR) flow.

About the Author

Vincent Huard received the B.S. (1996) in physics and the M.S. (1997) in electrical engineering from the Institut National Polytechnique de Grenoble (INPG). He worked for the CEA-Grenoble on the MBE growth of II-VI based doped heterostructures and their magneto-optical and electrical characterizations. He received his Ph.D. (2000) in physics from the university of Grenoble. In 2000 and 2001, he was a Visiting Scholar at the University of California, where he worked on devices made of ferromagnetic materials on top of semiconductors. In 2002, he joined Philips Semiconductors as a reliability engineer, working on oxide and device reliability. Since 2007, he is at STMicroelectronics, now serving as Device to Product Reliability manager, working on device and circuit reliability modeling and product qualification tests. His current research interests include NBTI, HCI and TDDB degradations both at wafer and product levels as well as Design for reliability. He authored and co-authored more than 140 regular papers, several invited papers and tutorials, held 9 patents and is serving as IRPS Management Committee member.

Sunday Tutorial Topic 4.1

FLASH RELIABILITY

Todd Marquart, Micron

Abstract

As flash memories continue to scale in density and dimension the reliability is converging with the field reliability requirements, making understanding of the reliability limitations of flash memories extremely important. This tutorial is an introduction and overview of those mechanisms, along with a basic understanding of operation of flash memory with emphasis on NAND floating gate memories. The primary reliability mechanisms and their interactions are covered along with example system level management techniques to deal with these mechanisms.

About the Author

Todd Marquart is a Distinguished Member of the Technical Staff at Micron Technology. He received his Ph.D. in inorganic chemistry from the University of Illinois, Urbana-Champaign with post graduate research at Sandia National Laboratories. He has been working in semiconductor reliability for over 17 years, the last 9 years with Micron Technology. At Micron he has been responsible for reliability analysis of NAND flash as part of Micron's Flash process R&D group. Recently he has undertaken work on the reliability of NAND based Solid-State-Drives (SSD) produced by Micron. He teaches semiconductor reliability and life-data-analysis at Micron and has been doing side research with Wes Fulton and Dr. Bob Abernethy on Weibull/life-data analysis.

Sunday Tutorial Topic 4.2

Emerging Memory Technologies

Matthew Marinella, Sandia

Abstract

In the not too distant future, the traditional memory and storage hierarchy of may be replaced by a single Universal Memory device integrated with the logic processor. Traditional magnetic hard drives, NAND flash, DRAM, and higher level caches (L2 and up) will be replaced with a single high performance memory device. The Universal, or Storage Class Memory (SCM) paradigm will require high speed (< 100 ns read/write), excellent endurance (> 10^{12}), nonvolatility (retention >10 years), and low switching energies (< 10 pJ per switch). The International Technology Roadmap for Semiconductors (ITRS) has recently evaluated several potential candidates SCM technologies, including redox RAM (ReRAM), spin transfer torque magnetic RAM (STT-MRAM), and phase change RAM (PCRAM). All of these devices show potential well beyond that of current flash technologies and research efforts are underway to improve the endurance, write speeds, scalability, and reliability to be on-par with DRAM. Performance, reliability, cost, and manufacturability will decide which emerging memory technology enables this major technological paradigm shift. This tutorial reviews the state of the art of these emerging memory devices with respect to performance and reliability, and evaluates them as Storage Class Memory candidates.

About the Author

Matthew Marinella is a Principal Member of the Technical Staff at Sandia National Laboratories in Albuquerque, NM, where he recently established and leads a research program in ReRAM and co-leads an advanced power electronics program. He is also the Chair of Emerging Memory Devices for the International Technology Roadmap for Semiconductors (ITRS). Prior to Sandia, Dr. Marinella worked as a CMOS Device Technology Development Engineer at Microchip Technology in Tempe, AZ. His research interests include emerging memory and logic devices, nanotechnology, advanced computing architectures, power electronics, and photovoltaics. Dr. Marinella has authored or co-authored over two dozen journal and conference publications, one book, chaired and organized conferences sessions, and has given invited talks in the areas of emerging devices and architectures and advanced power devices. He received his PhD in Electrical Engineering at Arizona State University under Prof. Dieter Schroder.

Sunday Tutorial Topic 4.3

On the Intrinsic Variability and Reliability of Solar Cells

Muhammad A. Alam, Purdue University

Abstract

Our ability to design integrated circuits despite variability of performance from one transistor to the next, and our ability to ensure reliability under broad range of operating conditions have been essential to the development of the semiconductor industry. The variability and reliability issues play even more critical role for the PV industry. While nobody wants a 10-year old iPhone, if a PV installation continues to produce power reliably 10-years after the warranty period, it is free energy that translates directly to 'return on investment'.

Although single crystalline silicon has long dominated the market for solar cells for its relatively high efficiency and high-degree of reliability, many companies are now exploring other (somewhat) less efficient material options (e.g., CdTe, a-Si) that offer improved cost/watt through significantly lower manufacturing cost. If the reliability challenges associated with these materials could be appreciated and addressed, the economic viability of these PV options could be improved dramatically.

The reliability issues of solar cells could either be extrinsic (e.g. glass-breakage, wiring fault, etc.) or intrinsic (e.g. light induced degradation, moisture-induced polymer breakdown, delamination, etc.). In this talk, I will discuss the physics and technological origin of five intrinsic reliability/variability concerns related to thin film solar cells: (i) shunt conduction, (ii) light- and stress-induced degradation, (iii) hot-spot generation, and (iv) polymer degradation and (iv) Na diffusion/incorporation. I will discuss the universality of the reliability issues across various technologies and discussion strategies developed to address them.

About the Speaker

MUHAMMAD ASHRAFUL ALAM is a Professor of ECE at Purdue University where his research and teaching focus on physics, simulation, characterization and technology of classical and novel semiconductor devices. From 1995 to 2001, he was with Bell Laboratories, Murray Hill, NJ, as a Member of Technical Staff in the Silicon ULSI Research Department. From 2001 to 2003, he was a Distinguished Member of Technical Staff at Agere Systems, Murray Hill, NJ. He joined Purdue University in 2004. Dr. Alam has published over 150 papers in international journals and has presented many invited and contributed talks at international conferences. He is a fellow of IEEE, APS, and AAAS, a Distinguished Lecturer of Electron Device Society, a member of Sigma Xi, and the recipient of 2006 IEEE Kiyo Tomiyasu Award for contributions to device technology for communication systems.