IRPS 2014

IEEE International Reliability Physics Symposium

Sunday Tutorial Presentations

June 1, 2014

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S1.2: Bias Temperature Instability in HKMG MOSFETs: Characterization, Process Dependence, DC/AC Modeling and Stochastic Effects

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Sunday Tutorial Topic 1.1

CMOS Front-End Reliability (TDDB)

James Stathis, IBM Research Division

Abstract

Dielectric breakdown is one of the most important fundamental issues in silicon technology. Breakdown exhibits a range of complex behavior and is inherently statistical. New challenges include the introduction of new materials such as high-k and low-k dielectrics with increasing process complexity. This tutorial will provide an introduction to topics including measurement methods such as constant-voltage stress and ramped-voltage stress, physics-based models of breakdown and the associated voltage acceleration laws, Weibull- and non-Weibull breakdown statistics, and post-breakdown behavior. Examples will be drawn from SiON/Poly-Si and high-k/metal-gate technologies.

About the Author

Jim Stathis has a Ph.D. in Physics from the Massachusetts Institute of Technology. He is currently manager of reliability research and electrical characterization at the IBM T. J. Watson Research Center. He is the author or coauthor of more than 140 research papers and over 70 invited talks on defects, wearout, and breakdown. He was the Technical Program Chair for IRPS 2009 and General Chair for IRPS 2011. He is an Associate Editor of the journal Microelectronics Reliability, a Fellow of the American Physical Society, and an IEEE Fellow.

Sunday Tutorial Topic 1.2

Bias Temperature Instability in HKMG MOSFETs: Characterization, Process Dependence, DC/AC Modeling and Stochastic Effects

Souvik Mahapatra, Indian Institute of Technology Bombay

Abstract

A common framework involving mutually uncorrelated trap generation and trapping sub-components is introduced to explain NBTI and PBTI degradation in HKMG MOSFETs. The framework can explain experimentally observed impact of different HKMG processes on BTI, including that of IL scaling and Nitridation. The underlying trap generation and trapping sub-components are independently verified by direct characterization techniques, and their relative impact on overall BTI is established for different HKMG processes. The similarities and differences between NBTI and PBTI mechanisms are highlighted using carefully designed HKMG process splits. A comprehensive physics-based model is established for prediction of time evolution of degradation and recovery during and after DC and AC stress at different bias and temperature, and AC stress at different frequency and duty cycle. The model can predict end-of-life degradation for DC and AC stress. The framework is extended to explain stochastic BTI observed in small area devices. The relative impact of process variability and BTI variability is discussed. Finally, a SPICE compatible compact model is introduced for macroscopic and stochastic BTI.

About the Author

Souvik Mahapatra received his PhD in Electrical Engineering from IIT Bombay, Mumbai, India in 1999. During 2000-01, he was with Bell Labs, Lucent Technolgies, Murray Hill, NJ, USA. Since 2002 he is with the Department of Electrical Engineering at IIT Bombay and currently holds the position of full professor. His research interests are in the area of CMOS logic gate stacks - scaling and reliability, and flash memory devices. He has published more than 150 papers in peer reviewed journals and conferences, delivered invited talks in major IEEE conferences including the IEDM, delivered tutorials in IEEE IRPS, and served as a reviewer and committee member of many IEEE journals and conferences. He is a fellow of the Indian National Academy of Engineering, senior member of IEEE and a distinguished lecturer of IEEE EDS.

Sunday Tutorial Topic 1.3

Hot-Carrier to Cold Carrier Issues in Nanoscale CMOS Nodes: from Energy Driven to Multiple Particle Regime

Alain Bravaix, ISEN, REER-IM2NP

Abstract

The evolution of the HC phenomena towards cold carrier (CC) interaction mechanisms poses new challenges in the determination of the proper modeling of generated defects at low voltages from devices to circuits reliability statements. The tradeoff between performances and reliability with the rise of the operating temperature becomes tricky as the classical HC picture has to be modified to the energy driven formalism taking into account the scattering mechanisms and thermal effects in ultra-short channel which move to current driven damage in nanometer scaled MOSFETs. This tutorial focuses on the new requirements for advanced modeling of HC phenomena as a function of the scaled CMOS nodes. After a short recall of the classical HC damage (part I) composed of interface traps and charge trapping into the gate-oxide of MOSFETs which are still met in Input/Output (IO) devices well described by the lucky electron model (LEM) from thick ($T_{ox} \geq 7$nm) to medium range T_{ox} (3.2nm £ T_{ox} £ 5nm) where charge detrapping is implied, we will turn to decananometer MOSFET ($T_{ox} < 3.2$nm) using a unified energy driven formalism (part II) between high carrier energy, to high carrier density, as now CC damage results in a multiple particle (MP) degradation process thermally activated under multivibration excitation of the passivated dangling bonds at the interface. This current driven CC damage allows transferring On/Off DC accelerating damage to AC ageing involved in logic cells using useful age(t_s) functions, for any pulse configurations which are readily checked between experiments and modeling (part III) where the HC implication is presented with some examples from digital to analog applications. As an increasing HC damage is observed in PMOS cumulated to the NMOS one, this suggests additional thermal effects by Negative Bias Instability NBT damage, where both degradation are closely interlinked during digital operation (part IV). This can be described through a self-heating (SH) approach which is found much larger in 28nm fully depleted silicon on insulator (28FD) high-K metal gate(HKMG) technologies than both 28nm HKMG silicon bulk (28LP) and 40nm (40LP) with SiON dielectric CMOS nodes. A complete modeling is finally applied to NMOS and PMOS devices that can be further extended to 28FD HKMG (part V) where the transfer to thermal modeling can be obtained as a function of the static power. This offers a complete comparison between 28LP silicon bulk and 28FD SOI submitted to MP degradation process with the interplay of thermal effects, opening new perspectives for an accurate HC to CC reliability determination in actual and future nanoscale CMOS nodes.

About the Author

Alain Bravaix graduated from the University of Sciences of Paris and joined the R&D research laboratory of BULL S.A. in 1988. He received the Ph.D. degree in microelectronics in 1991. From 1991 to 1993, he worked on gate-oxide nitridation optimization as a post doctorate fellowship in the Solid-State Physics Research group of the Institut d'Electronique et de Microélectronique du Nord (IEMN). Since 1994 he is developing research activities and as a professor for Engineering and Master degrees at the Institut Supérieur d'Electronique et du Numérique (ISEN-Toulon) and at the Institut Matériaux Microélectronique Nanosciences de Provence (IM2NP) UMR 7334. He worked for ST Microelectronics Crolles since 1994 on the reliability and optimization of CMOS and BICMOS technologies. This led in 2014 to the creation of a "Radiation Effects and Electrical Reliability (REER) joint Laboratory" in collaboration with ST Microelectronics Crolles and Aix Marseille University (AMU). His research interests cover device physics to circuit reliability, electrical characterization techniques to fast switching experiments (on the fly), optimized processing for novel and ultra-small CMOS nodes scaled towards 22-14nm FDSOI nodes challenging FinFET technologies. D^r Bravaix is a member of the IEEE Electron Devices and Reliability Society and became IEEE Senior member in 2012. He is author or co-author of more than 150 technical papers with several tutorials and invited papers in these fields.

Sunday Tutorial Topic 1.4

CMOS FEOL Reliability in Advanced Nodes – A Foundry Perspective

Biju Parameshwaran, GLOBALFOUNDRIES

Abstract

Innovation in the semiconductor industry has led to relentless technology scaling in the past four decades. This tutorial will provide an overview of reliability challenges as the industry continues to scale technology. With High-K Metal Gates replacing the conventional SiON Poly gate stack, new challenges have been introduced in FEOL reliability. This tutorial will delve in some detail on these new challenges examining some of the reliability mechanisms in some detail and on the close co-optimization required between technology development and reliability to overcome these challenges. Product designs squeezed from short development schedules and time-to-market requirements have to deal with increased design constraints coming from reliability mechanisms, in addition to those from a host of phenomena related to technology scaling. Highlight in some detail will be provided on the circuit impacts of reliability and efforts to develop methodologies to incorporate upfront reliability margining in early design phases. With a transition from IDM to foundry manufacturing, challenges for reliability qualification and reliability enablement from a foundry perspective will also be presented.

About the Author

Biju Parameshwaran received Bachelor of Technology (Hons.) in Metallurgical Engineering from Indian Institute of Technology, Kharagpur, India, and his M.S. in Materials Science from Arizona State University. He joined Cypress Semiconductor, San Jose in 1995, working on process development and transfer of a wide range of technologies like SRAMs, Flash, SONOS, HP SiGe-BiCMOS, and at Silicon Magnetic Systems (a subsidiary of Cypress Semiconductor), San Jose, on Magnetic RAMs from 2002 to 2005. He joined AMD in 2005 in the Logic Technology Division as a reliability-design interface, and has worked in other areas like design rule and mask Boolean formulation, SRAM modeling and DFM. He has been with GLOBALFOUNDRIES since its inception in 2009, currently managing the FEOL reliability group in the Quality and Reliability Engineering Department in Malta, NY and Sunnyvale, CA. He and his team are responsible for wafer level reliability qualification, customer reliability enablement, and reliability methodology development for advanced technology nodes.

Sunday Tutorial Topic 2.1

GaN Device Reliability

Matteo Meneghini, University of Padova

Abstract

Thanks to the low on-resistance, high thermal conductivity, and high breakdown field, GaN-based HEMTs are expected to find wide application in the power electronics field. However, the high electric fields and temperatures reached during operation may favor a number of parasitic and lifetime-limiting mechanisms; more specifically: (i) charge trapping may be responsible for the so-called current (or Ron) collapse, i.e. the dynamic decrease in drain current induced by the exposure to high drain bias levels. To improve the performance of the devices, it is important to develop methods for trap characterization, and to investigate how the epitaxial quality and device process can impact on trap density. (ii) off-state stress may induce a severe degradation of the devices, resulting in an increase in gate-drain or source-drain leakage current, or in the catastrophic failure of the transistors; (iii) the breakdown voltage of these devices is often lower than the theoretical limit, due to several physical mechanisms (vertical leakage, punch-through, DIBL, gate-drain breakdown, impact ionization …) that need to be separately investigated; (iv) when devices are operated in on-state, hot-electrons may induce a measurable degradation, due to the trapping of negative charge in the gate-drain access region (in the passivation or in the semiconductor layer). This tutorial reviews the physical mechanisms that limit the performance and the reliability of GaN-based HEMTs for power applications; during the presentation, we will also discuss methods for improving the performance and reliability of the transistors. A critical review of the most recent studies on these topics will be presented.

About the Author

Matteo Meneghini received the Ph.D. from the University of Padova, Italy, working on the optimization of GaN-based optoelectronic devices (LEDs and lasers). He is currently assistant professor at Department of Information Engineering, University of Padova. During his career he has extensively worked on the reliability and parasitics of GaN-based semiconductor devices for application in the RF, power electronics and optoelectronics fields: his research is mainly focused on the understanding of the physical mechanisms that limit the performance and the reliability of GaN-based LEDs, lasers, and HEMTs. Within his activity, he has cooperated with a number of research institutes and companies, including the University of California at Santa Barbara, the University of Cambridge, University of Wien, IMEC, OSRAM-OptoSemiconductor, Panasonic Corporation, Fraunhofer IAF, and Universal Display Corporation. He has been also involved in several Italian, European and International Research Projects. He presented more than 200 contributions in international journals and/or conferences. He co-authored 8 invited papers on international journals, and has been invited to speak at several international conferences. Meneghini was also personally invited as a Tutorial Speaker to international conferences (including IEEE IRPS, ESREF, IIRW). He is also co-inventor of a number of patent applications. Meneghini is a Senior Member of IEEE and a member of the SPIE. He – together with his colleagues - won several best paper awards at international conferences (including ESREF 2009, IWN 2012, ESREF 2012).As a recognition for his research activity at the University of Padova, he received the “Carlo Offelli Award 2008” (best young researcher of the Department of Information Engineering for year 2008). Matteo Meneghini is a member of the following committees: IEEE International Electron Device Meeting (IEDM), ESSDERC 2013 Technical Program Committee (TPC), ESSDERC 2014 Technical Program Committee (TPC), Technical sub-committee of ESREF (the European Conference on Reliability of Electron Devices). He has been a member of the local organizing committee of the 31th Workshop on Compound Semiconductor Devices and Integrated Circuits, May 20-23th, 2007 Venice, Italy, of the 17th European Heterostructure Technology Workshop, HETECH 2008, Venice, Italy, November 2-5, 2008, and of the 14th International Symposium on the Science and Technology of Lighting, Como Lake, June 22-27, 2014. He is in the advisory board of the conference LED Professional Symposium.

Sunday Tutorial Topic 2.2

Addressing Middle-of-the-Line Reliability Issues

Fen Chen, IBM Microelectronics

Abstract

This tutorial will cover emerging Middle-of-Line (MOL) reliability for FinFET and advanced planar MOSFET. MOL dielectric breakdown in advanced CMOS technology nodes has emerged as one of the most challenging reliability mechanisms since 32nm technology node due to the aggressive shrinking of the gate to diffusion contact pitch. Complicated process control such as PC-CA overlay, critical dimension (CD), and line-edge roughness (LER), rapid adoptions of new materials such as metal gate, stress liner, and copper contact, together with new device configurations such as epitaxial source/drain and FinFET further exacerbate the PC-to-CA dielectric breakdown problem. Elevated PC-to-CA leakage and early breakdowns could result in product yield loss and functional stress failure if MOL process is not optimized. In this tutorial, how to conduct a comprehensive evaluation of MOL PC-to-CA reliability, including novel test structure design, new big stress data generation and analytics technique, and new failure rate projection methodology will be discussed. MOL PC-to-CA spacer dielectric is commonly convoluted with multiple variables present in the data. The traditional method of stressing one DUT per die or multiple DUTs per die, without careful data deconvolution, is incapable of addressing current complex MOL PC-to-CA breakdown challenges. Therefore, a new big data generation method plus an analytics procedure is proposed to soundly evaluate MOL reliability. Based on our new big data and analytics method, a new diagnostic reliability concept is for the first time proposed for a comprehensive MOL process diagnostics and more accurate MOL reliability failure rate determination. Furthermore, based on extensive wafer-level stress and product level stress data, it was found that multiple PC-to-CA failure modes could exist and act in concert or separately to determine the ultimate product reliability. In this tutorial, various intrinsic PC-to-CA geometry induced failure modes and various process issue induced extrinsic failure modes will also be discussed in details. It will be emphasized in this tutorial that both intrinsic minimum insulator spacing and extrinsic defects should be carefully evaluated during technology qualification in order to ensure a robust PC-to-CA reliability at product level.

About the Author

Fen Chen received his Ph.D. degree in Electrical Engineering in 1998 from University of Delaware. From 1997 to 1998, he was with IBM System Group at Rochester, MN and Intel Component Research at Santa Clara, CA as a graduate intern working on system stress and IC interconnect reliability. He joined IBM Microelectronics at Essex Junction, VT in 1998 and has worked on semiconductor technology reliability issues since that time. During the past several years he has focused on low-k ILD TDDB, MOL PC-to-CA dielectric, MOL CA/silicide contact robustness, and 3Di TSV related dielectric reliability issues for various IBM and IBM Alliance development programs at 65nm, 45nm, 32nm, 22nm, 20nm, and 14nm. He holds more than 40 patents and has published over 50 technical papers. He currently is the chairman of JEDEC 14.2 wafer level reliability committee.

Sunday Tutorial Topic 2.3

Process Integration & Variability interaction with BEOL Reliability

Oliver Aubel, GLOBALFOUNDRIES and Martin Gall, Fraunhofer IKTS

Abstract

In former technology nodes, extensive and detailed reliability investigations were a central part of process qualification efforts, but mainly served as verification for the technology development success only. Since the 65nm technology node or latest at 45nm, the reliability characterization has become a major part of the technology development itself. It has a strong impact on the choice of the process options or necessary process changes. Future technology nodes are very challenging with respect to meeting reliability targets. Only with carefully chosen unit process options and an optimized balance between design and reliability demands, technology nodes of 28nm dimensions and beyond can be successfully introduced. In this tutorial, the interaction between process options and reliability requirements will be covered and several critical aspects to ensure BEOL reliability in 28nm technology nodes and beyond will be discussed. A common key work for intrinsic reliability performance loss is for example the electromigration crisis. Here, the reliability robustness is reduced due to scaling, leading to reduced critical void volume yielding a resistance increase failure. Aspects such as barrier via side wall coverage or potential etch back issues are not covered in this physics-based model and need to be addressed. The tutorial will focus on the process-related items which overlay the intrinsic reliability performance.

About the Author

Dr. Oliver Aubel has earned his diploma (M.S.) in electrical engineering with focus on microelectronic engineering from the University of Hannover (Germany) in 2000. In early 2004, he finished his Ph.D. studies at the same university with a focus on highly accelerated electromigration testing. Immediately thereafter, he joined GLOBALFOUNDRIES (formerly AMD) (Germany) as a reliability engineer for interconnect reliability. In his early years at GLOBALFOUNDRIES he was assigned to the IBM technology development alliance at the Burlington site in Vermont, US (2004-2005). After returning to Germany, he managed the reliability teams of Fab1, Germany in different configurations and is now responsible for global quality and reliability alignment and roadmap development for all GLOBALFOUNDRIES sites. He underlines his knowledge of process and reliability interaction with several patents and his major contribution to about 80 international publications.

Dr. Martin Gall is currently department head of Materials and Reliability for Micro- and Nanoelectronics at the Fraunhofer Institute for Ceramic Technologies and Systems in Dresden, Germany (FhG IKTS). He received the title of Diplomphysiker (M.S. in physics) from the Rheinisch-Westfaelische Technische Hochschule Aachen, Germany, in 1992, and a Ph.D. in materials science and engineering from The University of Texas at Austin, USA, in 1999. He joined the Motorola Semiconductor Division (later to become Freescale Semiconductor) in 1995 as an engineer and has since been working in the area of backend reliability, mainly addressing issues with electromigration, stress-induced voiding, and time-dependent dielectric breakdown. From 2002 until 2009, he managed the interconnect reliability team in Freescale Semiconductor's Technology Solutions Organization, mainly focusing on implementation of advanced, low-k dielectrics in the 65, 45, 32 and 22 nm nodes. From 2007 until 2009, he was assigned to the IBM/Freescale Semiconductor Technology Alliance in Yorktown Heights and Hopewell Junction, NY. He relocated back to Europe in 2010 to join GLOBALFOUNDRIES, Dresden, Germany, and subsequently the Fraunhofer Research Society in 2011. He has (co)authored about 60 papers and serves as a technical committee member and reviewer for leading conferences and journals.

Sunday Tutorial Topic 2.4

Organic Devices Reliability

Andrea Cester, University of Padova

Abstract

Since the past few years, organic devices are gaining much attention of many research groups, academic institutions and companies. In many aspects organic devices have reached the performances of their inorganic counterparts. Besides, they can be manufactured at extremely low costs. In fact, organic semiconductors can be deposited or grown at very low temperature, thus requiring very small thermal budgets. This also makes organic semiconductors compatible with plastic substrates, which are flexible, lighter, less expensive and more robust than glass. Furthermore many deposition techniques, such as inkjet or roll-to-roll printing, are well suited to large area devices, which is a very desirable feature especially for solar cells and display. Despite all the advantages, organic devices still have some drawbacks. In particular, being relatively novel devices, their reliability and stability is still under investigation. Besides, organic compounds might be very sensitive to ultraviolet or even blue light coming from the sun, as well as high temperature, humidity adsorption, etc. These issues must be addressed for a successful commercial application of these devices. This tutorial starts with a review the fundamentals of organic semiconductor, with particular emphasis on the most important differences between organic and traditional semiconductor materials. Then an overview of the most important organic devices will be presented, including electronic, optoelectronic, photovoltaic devices and sensors. The main part of this tutorial will be focuses on the most critical reliability and stability issues of organic devices and their applications. Some case studies of the most recent reliability reports on these topics will be presented.

About the Author

Andrea Cester received the Ph.D. in Electronics and Telecommunications Engineering from the University of Padova, working on the reliability of ultrathin gate oxide employed in the deep submicron CMOS technology for ULSI applications. On December 20, 2002 he joins the Department of Information Engineering of the University of Padova as Assistant Professor. During his career he has extensively worked on the characterization, the reliability, and the modeling of electronic devices, ranging from the deep-submicron bulk and SOI CMOS devices, non-volatile memories, organic semiconductor devices, III-V semiconductor, RF-MEMS, and photovoltaic devices. His research activity is mainly focused on the understanding of the physical mechanisms that limit the performance and lifetime of semiconductor devices, the ionizing radiation effects on devices and circuits, the modeling of device and degradation mechanisms. From 2008, he started a new research line and a new research laboratory in the Microelectronic group of the University of Padova focused on the characterization, reliability and modeling of organic electronic, optoelectronic, and photovoltaic devices. Within his activity, he has cooperated with a number of research institutes and companies, including ST Microelectronics, Universal Display Corporation, IMEP-ENSERG of Grenoble, Center for Hybrid and Organic Solar Energy (CHOSE), University of Rome “Tor Vergata”, Slovak University of Technology, University of Purdue, CEA-LETI, Sandia National Lab., IMEC INFN, CERN, CNR-ISMN. He has been also involved in several Italian and European Research Projects. Andrea Cester is Senior Member of the IEEE. He is author or co-author of more than 150 publication on International journals and conferences (three on invitation) and 2 book chapters. One of these works obtained the Best Student Paper Award (ESSDERC 2000). Andrea Cester has participated to several committees, including IEEE - International Reliability Physics Symposium - (IRPS), IEEE - Nuclear and Space Radiation Effects Conference (NSREC), Conference on Radiation and its Effects on Components and Systems (RADECS), European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), European Solid State Device Conference (ESSDERC).

Sunday Tutorial Topic 3.1

Unified Approach for Simulation of Statistical Reliability in Nanoscale CMOS Transistors from Devices to Circuits

Asen Asenov, Gold Standard Simulations, Ltd., University of Glasgow

Abstract

The scaling down of the CMOS transistors necessitates the adoption of Reliability-Aware circuits and systems design methodology. Indeed, charge trapping related issues such as random telegraph noise (RTN) and bias temperature instabilities (BTI) are major threat to SRAM yield and endurance. It is well understood that the interplay between statistical variability, introduced by the discreetness of charge and granularity of matter, and the discrete oxide charge trapping related degradation in transistors necessitates the interpretation of their performance- and reliability- figures of merit as time dependent stochastic variables. Corroborated by a surge of new experimental evidences an important paradigm shift has identified the discrete charge trapping/de-trapping in the gate oxide as unique phenomenon underlying both RTN and BTI. In this tutorial we will present the recent advances in the simulation of statistical variability effects from device to circuit level. The simulations are based on 3-D Kinetic Monte Carlo simulations technology that follow trapping/de-trapping history of large ensembles of microscopically different transistors, accounting for the discrete nature of both doping and oxide traps and reproducing the stochastic process ruling the discrete charge injection into the gate oxide. The results of the physical simulation of the time dependent evolution of the statistical variability are than captured in accurate time dependent statistical compact models. As a result accurate statistical circuit simulation can trace the statistical impact of the degradation on the functionality of the underlying circuits and systems. This allows the concepts of Design-Technology Co-Optimization (DTCO) to be extended into the reliability domain. We will illustrate the above comprehensive simulation approach with examples of statistical reliability simulations in contemporary and future bulk and FDSOI MOSFETs and FinFETs. We will use statistical SRAM simulation to illustrate how the results of the physical simulations can be used to evaluate the resilience of the corresponding SRAM circuits and to reduce the design margins.

About the Author

Asen Asenov (FIEEE, FRSE) is a founder and CEO of Gold Standard Simulations (GSS) Ltd. (www.goldstandardsimulations.com). GSS is the leader in physical simulation of statistical variability, statistical compact model extraction and generation technology and statistical circuit simulation. The GSS customers include foundries, IDMs, fables companies and design IP startups. Asenov is also a Director of SureCore, Ltd, a green SRAM design IP start-up company. As a James Watt Professor in Electrical Engineering and Leader of the 30 members strong Glasgow Device Modelling Group (http://web.eng.gla.ac.uk/groups/devmod/) Asenov directs the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. Asenov has more than 690 publications and more than 170 invited talks in the above areas.

Sunday Tutorial Topic 3.2

Reliable Design of CMOS Circuits in Scaled CMOS Technology

Kaushik Roy, Purdue University

Abstract

Scaling of technology and the use of high-k dielectrics has led to increased variability in circuit parameters, due to process and aging effects. In this tutorial, I will first present impact of parameter variations on both logic and memory circuits. Then I will present error resilient run-time and design time techniques to achieve high yield while keeping power consumption within bounds.

About the Author

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, for three years before joining the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. His research interests include spintronics, device-circuit co-design for nano-scale Silicon and non-Silicon technologies, low-power electronics, and reliable CMOS design. Dr. Roy has published more than 600 papers in refereed journals and conferences, holds 15 patents, graduated 60 PhD students, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill). Dr. Roy received the National Science Foundation Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, Purdue College of Engineering Research Excellence Award, Humboldt Research Award in 2010, 2010 IEEE Circuits and Systems Society Technical Achievement Award, Distinguished Alumnus Award from Indian Institute of Technology (IIT), Kharagpur, Fulbright-Nehru Distinguished Chair, and several best paper awards in conferences and IEEE journals. Dr. Roy was a Purdue University Faculty Scholar (1998-2003). He was a Research Visionary Board Member of Motorola Labs (2002) and held D.J. Gandhi Distinguished Visiting faculty at Indian Institute of Technology (Bombay). He has been in the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, IEEE Transactions on VLSI Systems, and IEEE Transactions on Electron Devices.

Sunday Tutorial Topic 3.4

Single Event Effects Modelling across Various Design Abstraction Levels

Enrico Costenaro, Dan Alexandrescu, iROC Technologies

Abstract

Hardware is intrinsically unreliable. Particularly, perturbations induced by Single Event Effects may cause system downtime, data corruption and maintenance incidents. Thus, the SEEs are a threat to the overall system reliability performance causing engineers to be increasingly concerned about the analysis and the mitigation of radiation-induced failures, even for commercial systems performing in a natural working environment. The SEEs are physical phenomena, strongly dependent on technological process and design implementation. On the other end of the scale, any SEEs-induced faults have a potential for causing system-wide consequences. Thus, any Soft Error Rate (SER) analysis approach will require a multitude of competencies, solutions, tools and methodologies. This lecture presents an overview of the analysis of Single Event Effects in complex ASICs from process aspects to system-wide consequences. The study relies on a complete approach that integrates tightly with the design flow, enabling the reliability engineer to closely support the circuit designers in order to improve the overall Soft Error Rate of the system with the firm goal of improving customer experience when using high availability products. Dealing with all these subjects, this lecture hopes to improve the SER awareness in the electronic design field and to offer practical solutions when dealing with these problems, in helping both SER analysis and improvement efforts.

About the Author

Enrico Costenaro is the SoCFIT Product Manager at iROC Technologies; He works on the specification and development of EDA Tools for Soft Error Rate Analysis. His main interests include several aspects of the computer-aided design of digital integrated circuits and systems, with particular emphasis on soft error rate assessment and optimisation, and testing. Lately he has focused his efforts on the study and development of methodologies, algorithms and tools for reliability estimation and optimisation of systems described at various levels of the design flow. Enrico also participates to the research and development efforts of the company in the context of international & regional collaborative R&D projects. Additionally, he has published a number of research papers in journal and in the proceeding of international conferences.

Sunday Tutorial Topic 4.1

Reliability Qualification Strategies

Fred Kuper, NXP Semiconductors

Abstract

Every product to be delivered needs to be qualified to be reliable for its intended use. The main focus of IRPS, physics of failure mechanisms, is the basis of understanding reliability of products, but for an effective qualification program, reliability engineers need to translate fail mechanisms to impact during use conditions and relate this to required reliability stress tests and durations. In this tutorial it is explained what a qualification strategy is. Important elements that will be explained are the mission profile, the expected risks and the actual validation of the reliability of the product or technology. This physics based approach is called Robustness Validation and is used more and more for example in automotive. We will talk about significance of a qualification, obtaining mission profiles, the use of the reliability knowledge matrix, how to calculate test durations equivalent to mission profiles, and more.

About the Author

Fred Kuper received his M.Sc degree from the University of Twente and his PhD degree from the University of Groningen, both in The Netherlands. In 1987 he joined Philips Semiconductors (now NXP Semiconductors) and worked in a number of reliability related engineering and management functions. For his IRPS 1996 paper on the relation between yield and reliability he received the outstanding paper award. From 1998 to 2011 Fred Kuper was an extraordinary professor at the University of Twente in the field of Integrated Circuit Reliability. In 2002 he moved from the 8” wafer fab to an automotive business to become quality manager. Since 2008 Fred holds an automotive quality and reliability specialist position within the Business Unit Automotive of NXP Semiconductors.

Sunday Tutorial Topic 4.2

Reliability and Failure Analysis of Automotive Semiconductors

Noburu Nose and Akira Mikami, Toyota Motor Corporation

Abstract

Many electronic components are installed in the latest automobiles for the power control system and the body control system, etc. and a large number of semiconductors are installed in automobiles as a result. It is required that automotive semiconductors have high reliability. And the failure analysis technology is indispensable to achieve the high reliability. In this tutorial, the importance for quality improvement of automotive semiconductor, reliability and failure analysis for the automotive semiconductors will be explained.

About the Author

Noboru Nose works in the Electronics Development Div.3 of Toyota Motor Corporation for 25 years. After 10 years' experience in the development of assembly technology for semiconductor, I have been involved in reliability technology for automotive semiconductor.

Akira Mikami works in Electronics Development Div.3 for Toyota Motor Corporation. After the experience of the development of analysis technologies for various devices including semiconductors, lithium ion batteries, and fuel cells etc. in an electrical manufacturer for more than 20 years, I have been involved in the development of failure analysis for semiconductors in Toyota Motor Corporation.

Sunday Tutorial Topic 4.3

Space Reliability

Yuan Chen, NASA

Abstract

The reliability challenges for space missions are unique, mainly because of the space environment, the one-of-a-kind space systems, and the high level of reliability requirements. The tutorial is to go through the uniqueness of the space reliability challenges, space technologies, fundamental approaches and processes to ensure mission assurance, and some comparison to commercial industry. The tutorial is focused on design and reliability challenges from electronics perspective.

About the Author

Dr. Yuan Chen is currently a senior technical member with the Electronic Systems Branch, NASA Langley Research Center, Hampton, VA. She has been supporting a number of flight projects, research and technology projects, formulation studies and trade studies. Her research area is on the development and implementation of new technologies for space applications and their reliability qualification and mission assurance methodologies. Dr. Chen is the lead of the NASA EEE Parts Community of Practice and a member on the NASA Engineering and Safety Center (NESC) Avionics Technical Discipline Team, serving as a deputy to the NESC Avionics Technical Fellow. Prior to joining NASA Langley Research Center, she was a senior technical member with Jet Propulsion Laboratory (JPL) and a member of technical staff with Bell Labs, Lucent Technologies. Dr. Chen received her Ph.D. degree in reliability engineering from the University of Maryland at College Park, Maryland, in 1998, with a Graduate Fellowship from the National Institute of Standards and Technologies (NIST). She is a senior member of IEEE and an editor of IEEE Transactions on Device and Materials Reliability. She is also a senior member of AIAA and a member on AIAA Computer System Technical Committee.

Sunday Tutorial Topic 4.4

Product Reliability Seminar

Stuart Douglas and Ajay Kamath, Google [X]

Abstract

Reliability is the ability of a system to function as desired at a specific moment in time and stress. In consumer electronics, the system is a device which can be used often like a mobile phone or laptop, or more infrequently like a single task gadget. The effect of time on a product's reliability is different for each of these devices, but the effect of stress may be similar. In this tutorial, the presenters will discuss how system reliability can be affected by time and stress and a path to develop a reliable consumer electronics device. Consumer electronics are designed for an expected 3-5 year lifetimes with acceptable cumulative failure rates. Sample sizes into the hundreds of devices can be necessary to establish high reliability of a component. This tutorial attempts at establishing a path to reach a desirable system reliability, but the methods presented may not meet the needs of all programs and should be used as a way to prevent pitfalls by inexperienced programs.

About the Author

Stuart Douglas is a Reliability Engineer at Google [X] working on special projects, including Glass and the Self Driving Car project. Before joining Google, he worked on several generations of Kindle E-readers and Tablets and led analysis into the reliability of glass displays at Lab126. Stuart's research includes test and analysis of MEMS and electronics packages, brittle materials and thin films, and large mechanical systems. His academic research has been featured in two keynote IEEE EuroSimE conferences and won a "Best Thesis" university award. Stuart has a B.S. in Aerospace Engineering and a M.S. in Mechanical Engineering from University of Maryland and is a graduate of The Center for Advanced Life Cycle Engineering.